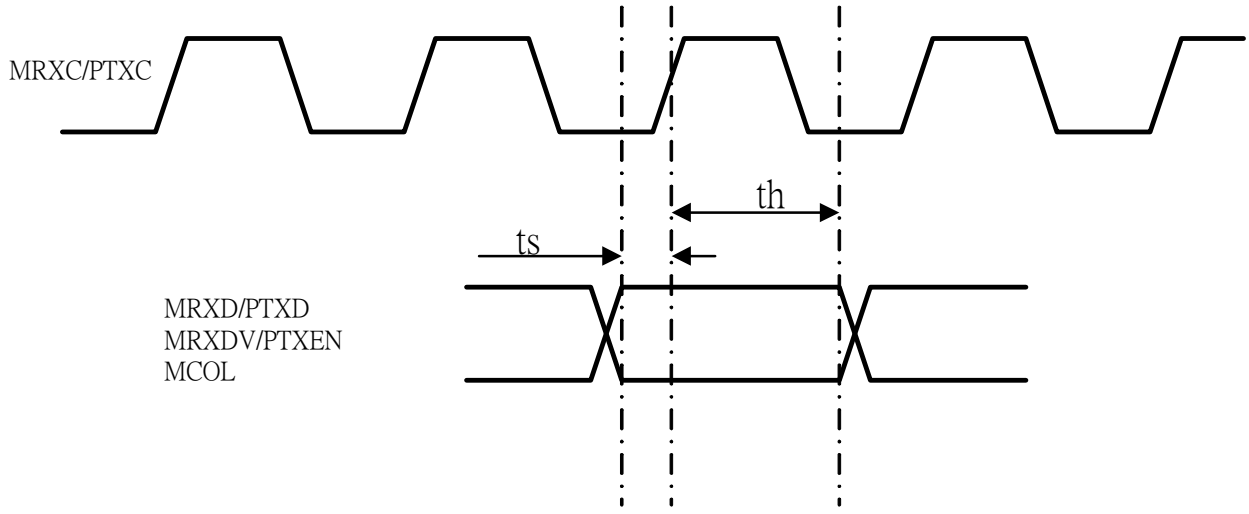
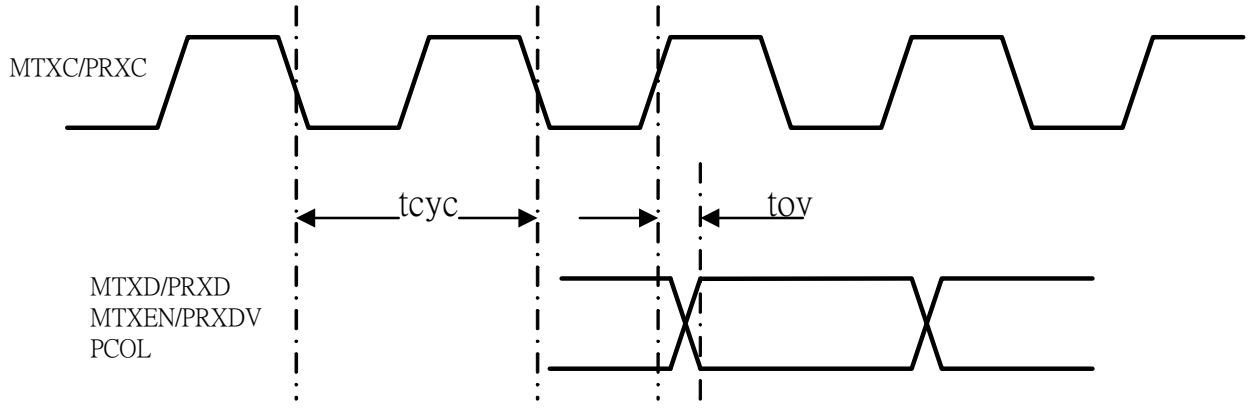
MII Timing of RTL8305SB

MII Timing			Min.	Typ.	Max	Unit
MRXD/PTXD, MRXDV/PTXEN, MCOL Setup time	ts	MRXD[3:0]/PTXD[3:0], MRXDV/PTXEN to MRXC/PTXC rising edge setup time	2			ns
MRXD/PTXD, MRXDV/PTXEN, MCOL Hold time	th	MRXD[3:0]/PTXD[3:0], MRXDV/PTXEN to MRXC/PTXC rising edge hold time	2			ns
MTXD/PRXD, PCOL to MTXC/PRXC delay	tov	Output delay from MTXC/PRXC rising edge to MTXD[3:0]/PRXD[3:0], PCOL	3	4.5	6	ns
100base PTXC, PRXC	tcyc	100base output MII clock cycle time		40±50 ppm		ns
10Base PTXC, PRXC	tcyc	10base output MII clock cycle time		400±50 ppm		ns



Receiving Data Timing (MRXD[3:0]/PTXD[3:0], MRXDV/PTXEN, MCOL)



Transmission Data Timing (MTXD[3:0]/PRXD[3:0], MTXEN/PRXDV, PCOL)

Sep. 5, 2002